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(54) IMPROVEMENTS IN DIGITAL DATA PROCESSING APPARATUS

(71) We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a corporation organized and existing under the laws of the State of New York in the United States of America, of Armonk, New York 10504, United States of America do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to improvements in digital data processing apparatus and particularly to improvements in systems for improving the detecting and correcting of errors in digital data when it is transferred from one location to another.

The invention finds particular use in digital data tape recording systems and may also be used with other magnetic recording media.

According to the invention there is provided digital data processing apparatus in which variable length strings of data signals are transmitted from one location to another in the form of segments of an equal predetermined length including a buffer store to store digital data signals in segment groups, first and second counters to keep a count of data signals entering and leaving the buffer store and means to determine the end of a string of data signals and to determine whether or not a complete segment has been transmitted depending upon the difference between the counts in the first and second counters.

In order that the invention may be fully understood a preferred embodiment thereof will now be described with reference to the accompanying drawings, in which:—

FIGURE 1 is a flow diagram of a digital data tape recorder embodying the invention;

FIGURES 2-1 and 2-2 are together a simplified logic diagram of buffer control and channel logic circuits used in the recorder of Figure 1;

FIGURES 2A and 2B are timing diagrams of signals used in the Figure 2-1 and 2-2 circuits.

Referring now to the drawings, Figure 1 shows in simplified form an I/O system for a magnetic tape recorder. Some connections have been omitted for the purpose of clarity.

The I/O system is under control of a microprocessor 38 which may be constructed as shown in United States Patent 3,654,617. Other known circuits 39 are used for sequencing control operation in cooperation with microprocessor 38. Circuits 39 perform a supervisory function. Data is received from and supplied to a data channel or CPU via cables 40, as well as control signals between circuits 39 or microprocessor 38. A scan-in/scan-out (scan) buffer 41 provides communication between cables 40 and main buffer 43 as sequenced by buffer controls 42.

Main buffer 43 preferably has a capacity of 32 bytes. It is basically a read-in/read-out count-controlled buffer wherein the count of a readout counter (CROC) associated with main buffer 43 forms one of the residual counts for odd/even checks. Main buffer 43 not only transfers signals to be recorded from scan buffer 41 through gating logic 44 to group buffer 45 for recording, but also receives data from read circuits 63 to be transferred over cables 40 to a connected CPU. Write control circuits 46 are supervised by microprocessor 38 and circuits 39 to generate the format on the recording tape. This operation is explained in detail in copending application 58902/73 (Serial No 1452968). Write error circuits 47 respond to signals received through gating logic 44 and the write control circuits 46 to generate error correction bits. Four register group buffers 45 and 48 each receive groups of four bytes of data (Group A), or three bytes of data plus a check bit byte (Group B),

each byte including an error detecting bit. These group buffers supply the four bytes in byte groups in parallel by bit form to encoder-gating (EG) circuit 49. The encoding portions of circuit 49 are constructed for converting the four bytes of data into five-bit storage code group values, each code group value lying along one of several tracks on the tape. EG 49 gates signals in a known manner for supplying serially arranged signals to recording circuits 50. Circuits 50 include the usual amplifiers and write compensation techniques, such as shown in United States Patent 3,503,059, and supply recording signals to transducer assembly or head 51 for recording such signals in tracks along the tape.

For reproducing signals previously recorded detectors 56 receive signals from head 51. Detectors 56 include the amplifiers and read compensation, as found in known digital data readback systems. Additionally, detectors 56 generate quality of readback signals which are supplied over cable 58 to deskewing apparatus 57, synchronously with data signals supplied over cable 59. Deskew apparatus 57 preferably may include 32 registers for accommodating about three segments of storage coded signals.

Deskew apparatus 57 supplies signals on a byte-by-byte basis to decode 60, constructed in accordance with United States Patent 3,624,637. Quality signals are supplied directly to read circuits 63. Decode 60 supplies the decoded signals of four data bytes, or three data bytes plus a check bit byte, to read circuits 63 where they are combined with the quality signals for error detection and correction purposes. In the event of an improper five-bit code group being received, decode 60 also supplies a corresponding quality-indicating signal referred to as a pointer. Additionally, format circuits 61 respond to the format groups, mark 1, and mark 2 for starting and stopping data signal transfers and the all-1's byte in five successive bytes to indicate end of data in a record. Circuits 61 supply such detected signal permutations to other circuits 39 and to microprocessor 38 for their supervisory action, as will become more apparent.

Read circuits 63 pass correct data signals in repeated bursts of seven bytes to main buffer 43 for retransmission over cable 40 to a connected CPU (not shown).

Special marker signals, and an all-1's byte can be generated in write control circuits 46 (or microprocessor 38) and supplied to encoder and gating circuits 49 over cable 55. Alternatively, they may be supplied through gating logic 44 for encoding in five lengths of five-bit run-length limited code groups.

Referring now to the drawings of Figure 2 as well as Figure 1. Bufferring occurs in the main buffer 43 (Figure 1 & Figure 2). The main buffer 43 may also be considered as a channel buffer and is count-in/count-out register type buffer well known in the digital data processing art. In buffer controls 42, the input counter is termed "CRIC" (channel read-in counter) 475, and the output counter is termed "CROC" (channel readout counter) 474. CRIC 475 controls all inputs to main buffer 43 during both writing or recording, as well as in readback operations. TAPE OP signal from microprocessor 38 on line 469 enables all circuits in MB 43 to operate. During recording, CRIC cooperates with write service logic circuits 460 to step data from scan buffer 41 into successively addressed registers in main buffer 43. CROC steps data from successively addressed registers in main buffer 43 through AND circuits 461, which constitute a portion of gating logic 44. AND circuits 461 are controlled by a gate-data signal.

During a readback operation, register 204 supplies signal bytes in bursts of seven through a set of A-O's 462 to main buffer 43 under control of CRIC. CROC, in cooperation with read service logic 463, transfers signals from successively addressed main buffer registers to scan buffer 41 for transmittal over channel bus-in (CBI).

Buffer controls 42 include priority circuits which give priority to write into main buffer 43 over readout. Buffering capacity in scan buffer 41, main buffer 43, and group buffer 45 is balanced to provide similar capability for signal transfer during either reading or writing.

First, a write operation is described, including the transfer of data signals from CBO (channel bus-out) through scan buffer 41, thence to main buffer 43 under control of write service logic 460. Transfers from main buffer 43 are controlled by buffer control 42 in conjunction with group buffers 45, 48, and write format circuits 46. The terminator portion (residual and check segments) of each data block is controlled by CRIC 475 and CROC 474 through the other logic circuits of buffer controls 42. During read, transfer of error corrected signals from register 204 continues through A-O's 462, main buffer 43, and scan buffer 40 under joint control of buffer control 42 and read service logic 463.

For a write data transfer, assuming that the initial selection of the controller has been made as shown in United States Patent 3,303,476, the control unit has been conditioned by establishing a recording or write mode of operation and is prepared to exchange data signals with a connected CPU as shown in United States Patent 3,582,906.

Scan buffer 41 has two buffer registers A and B respectively denoted by numerals 464

and 465. A register 464 receives signals from CBO and thence transfers such received signals over cable 466 through A-O's 462 to buffer write register 467. B register 465 is not used during the write operation. Register 467 retains one byte of data for recording in main buffer 43 for a short period of time to accommodate circuit delays.

A REG 464 is first loaded from CBO; then a write cycle is requested from main buffer 43 by write service logic 460. The buffer 43 write cycle includes readout of A REG 464 to register 467, while simultaneously permitting the write service logic 460 to request the next byte of data. These actions are repeated until completion of the write. Write service logic 460 initiates a buffer write cycle by sending write-data-ready signals over line 472 to main buffer 43 causing it to transfer A REG 464 signals to register 467 and to store the contents of register 467 at the buffer register address indicated by CRIC REG 473. CRIC REG 528 receives the input register number count or address from CRIC 475 each cycle just before CRIC 475 is incremented. Because of this relationship, CRIC REG 528 may have a count of one less than the contents of CRIC 475.

The write-request signal on line 472 is initiated by write service logic 460 responding to the connected CPU that the data on CBO has been stored in A REG 464. That is, the connected CPU/channel supplies either an SVCO (service out) or a DO (data out) signal as shown in United States Patent 3,582,906, respectively, over lines 476 and 477. These signals, when activated, initiate transfer into scan buffer 40 and upon initiation of a buffer write cycle, to register 467 and thence to main buffer 43.

The above-described write signal transfer follows after the initial selection has been completed and a recording operation has been commanded. Processor 38 responds supplying a signal indicating a write mode and that the control unit is tape operational (TAPE OP) and in write status. The TAPE OP signal, on line 482 and as indicated in Figure 2A, activates write service logic 460 by partially enabling AND circuits 481, 484, 485, and 486. These four AND circuits enable write service logic 460 to sequence transfers between the CBO portion of cable 40 and main buffer 43 in response to channel-supplied out tags SVCO and DO. Simultaneously with activating the write and TAPE OP signal, processor 38 supplies SVCI signal 487 (Figure 2A) over line 488. This SVCI signal travels through OR 489 to the SVCI line 490. During recording a block of signals, all subsequent SVCI signals 487A are supplied by AND 485, as will be described later. The initial SVCI 487 is always initiated by programs in microprocessor 38 for lodging the first request for a data byte in order to start write service logic 460 into the later-described sequences. At this time, the I/O control unit awaits transmission of the first byte of data over CBO portion of cable 40 with a coincident control or tag signal SVCO.

The connected CPU or channel responds to SVCI by sending one byte of data over CBO and simultaneously sending SVCO over line 476. Upon receiving SVCO over line 476, A-O 493 responds to SVCI active and SVCO active to generate service response pulse 494 traveling over line 495 to toggle SRT (service response toggle) 496 to the active state. SRT 496 memorizes and indicates whether the write signal transfer is under DO-DI or SVCO-SVCI control. This action stimulates write service logic 460 to transfer the byte of data on CBO into A REG 464, thence into MB 43. The service response pulse also resets the permit latch (PL) 515 to properly sequence the next in tag, SVCI or DI, as selected by the SRT 496 signal state.

Service response pulse 494 switches SRT 496 (service response toggle) from the inactive to the active state for supplying an output signal on line 497. With SRT 496 active and MBWT inactive, Exclusive-OR 513 is deconditioned (no active output signal is being supplied), thereby blocking AND's 485 and 486. Accordingly, SVCI from AND 485 and DI from AND 496 are inhibited. During this time, the CBO signals are lodged in A REG 464. AND 481 gates CBO signals to A REG 464.

Exclusive-OR 498 initiates transfer of the lodged signals from A REG 464 to MB 43. Exclusive-OR 498 is jointly responsive to SRT latch being active and the MBWT latch (main buffer 43 write cycle tally) being inactive to supply write data ready signal 499 over line 472 to buffer control 42 requesting that main buffer 43 be made available for receiving a byte of data to be recorded. Priority circuits in controls 42 defer any requests for data transfer from main buffer 43 to group buffer 45 for any buffer write cycle requests.

Write and TAPE OP signal on line 482 activates gates 573 to pass the signals on CBO to A REG 464.

SRT 496 and MBWT being in opposite stable states generate write data ready signal via Exclusive-or 498. This signal also activates AND 484 jointly with the write and TAPE OP signal to send a write cycle request signal via OR 509 to AND 539 for MB 43. AND 539 is activated to pass write cycle request signal only when MBF (main buffer full) latch 543 (later described) is reset. Main buffer 43 receives the write data ready signal and responds by sending

acknowledge signal MB43WR over line 511 indicating main buffer 43 has received write cycle request signal. MB 43 has its own internal clocking system (not shown) constructed in accordance with known memory system designs. MB 43 emits the MB43WR signal at the onset of its internal clocking cycle for transferring the A REG 464 signal contents through A-O's 462 to MB 43 input register 467. This action is accomplished by MB43WR activating the A1 portions of A-O's 462. A REG 464 is now free to accept the next byte from CBO. Main buffer 43 stores the signals in REG 467 in a register in MB 43 indicated by CRIC REG 528. Additionally, MB43WR signal triggers MBWT from the inactive to the active state. This action in write service logic 460 removes the write data ready signal from Exclusive-OR 498 while simultaneously activating Exclusive-OR 513 indicating that the next byte may be requested from the channel by supplying DI through AND 486 and OR 491. This action is indicated by the arrow extending from MB43WR signal to the leading edge of DI signal 492.

In the above-described instance, SVCI 487 being received from processor 38 in fact is removed by processor 38 in response to receiving SVCO. The programs in processor 38 are timed to allow the above-described circuits to receive the byte of data before SVCI is inactivated. In subsequent transfers, AND 485 supplies the SVCI signal and inactivates same in response to Exclusive-OR 513 removing its active output signal.

Write service logic 460 alternately activates AND 486 to supply data in (DI) and AND 485 to supply SVCI. Permit latch (PL) 515 and its input logic respond to the service response signal 494 and A-O's 478 analysis of the service tag signals to partially enable service response AND's 485 and 486, respectively, to activate either SVCI or DI for such data signal exchanges with the channel.

The analysis of the SVCO and DO signals is further controlled by AND 516 responding to the processor 38 generated "DI-DO enable" signal received over line 517 to pass the permit latch 515 signal to SDT latch. The line 517 signal indicates that the channel interface uses the SVCI, DI, and SVCO, DO signals. With AND 516 disabled, only SVCI and SVCO signals are used. The control signal on line 517 may be under microprocessor 38 program control, or from a plug, pinboard, etc., indicating the type of transfer tag signals required.

AND 516 passes permit latch 515 signal from line 522 to toggle SDT (SVCI-DI-trigger) between the S and D states, respectively indicating SVCI and DI signal exchanges. Initially, SDT is set to the S state in preparation for the first service response from the previously mentioned SVCI generated by processor 38. This signal toggles SDT to the D state after SVCO has been received, such that the A2 portion of A-O 478 passes the DO signal received over line 477 to AND 481 for the next succeeding data cycle. Upon the next channel-supplied service response, i.e., DO, SDT triggers to the S state enabling the A1 portion of A-O 478 to pass SVCO signal received over line 476. In this manner, the proper service response from the channel travels through A-O 478 to AND 481 for transferring CBO signal contents to A REG 464 and initiating transfer of the received byte to MB 43.

Additionally, A-O 478 supplies the inversion of its gated service response signal 494 to selectively set permit latch (PL) 515. In this regard, AND 521 jointly responds to the not service response signal on line 520 and the not A-O 478 signal to set PL 515. PL 515, being set, indicates that the out tag (SVCO or DO) corresponding to the next in tag (SVCI or DI) has become inactive so that the SVCI or DI in tag signals can be activated as indicated by the gating inputs to AND 485 or 486. PL 515 remains set until the next service response 494 occurs. Thus, PL 515 active output signal, supplied over line 522, enables AND's 485 and 486 to generate the SVCI or DI tags according to the state of the SDT latch.

The AND 481 output signal transfers data signals on CBO into A REG 464. This action represents the AND function combination of the write and TAPE OP signal on line 482, the output signal of A-O 478 as above discussed, and the service response signal on line 495.

The above-described circuit operations are basically asynchronous; that is, circuit delays, etc., determine the timing relationships. DC couplings, for example, between SDT and AND 481 are maintained as long as the input DC signals exist. Accordingly, the timings shown in Figure 2A are somewhat idealized and do not reflect variations in circuit delays, access delays to main buffer 43, and the like. These circuit timings are selected to accommodate signal rise, fall, and transfer times on CBO, as is well known in the circuit design arts.

From the above description, it is apparent how the data service portion for the second byte operates, that is, the DO/DI and service response, in order to transfer the second byte of data through A REG 464 to MB 43. AND 486 operates with in tag signal DI in the same manner that AND 485 operates with SVCI. These two AND's are constructed such that when the input portions are satisfied, then the corresponding in tag is activated.

The above description for transferring data bytes into main buffer 43 assumes no intervening transfer of data signals from main buffer 43 through gating circuits 44. In the event bytes are being transferred from main buffer 43 for recording, such buffer read cycles are interleaved between the above-described write cycles, the write into MB 43 having priority. Write service timings ensure that write cycles never occur on successive cycles, therefore allowing read cycles to be interleaved. Buffer controls 42 handle the priority of the write-read MB 43 transfer, as well as coordinating operation of main buffer 43. Additionally, the handling of the residual data bytes is determined by buffer control 42; that is, the last byte of data transferred from main buffer 43 during the readback operation to scan buffer 41 for retransmittal to CBI is determined by buffer controls 42 in accordance with the content of the residual counts referred to above.

Successive addresses in main buffer 43 for receiving bytes of data to be recorded from write REG 467 are tallied in CRIC (channel read-in counter) 475. Tally CRIC control 525 (a gating network) during a write operation is responsive to MB43WR signal received over line 511 from MB 43. Line 511 is active for each main buffer 43 write cycle so that each byte written into main buffer 43 increments CRIC 475. In the illustrated embodiment, CRIC is a five-digit binary counter for counting from 0 to 31 for the 32 register buffer 43. Each write cycle, just prior to the time CRIC is incremented, the five-bit count or register address is transferred to CRIC REG 528 which holds the count until the next byte of data is transferred to main buffer 43. CRIC REG 528 supplies the register address over cable 529 to main buffer 43 as the address at which the next byte of data is to be written. CRIC may also be incremented by each AND 481 signal, for example. Tally CRIC 525 is a gate passing the line 511 signal whenever allow CRIC latch 526 is active. Latch 526 is active during read forward at all times. During read backward, when compare circuits 524 indicate that the received count from register 591 and the address signals received over cable 676 are equal then CRIC is set.

The register addresses of main buffer 43 for readout purposes, i.e. transfer of data bytes to be recorded from main buffer 43 to group buffer 45, are determined by CROC (channel readout counter) 474. CROC 474 is incremented under control of tally CROC circuit 531, another gating network. Tally CROC 531 is responsive to MB 43 read cycle pulses (MB43RD) on line 532 to increment CROC 531 each time a byte is transferred and is read out from main buffer 43. The read cycle pulses from main buffer 43 are generated internally in MB 43 in accordance with known memory operations for monolithic semiconductive memories. In this regard, it should be noted that the initiation of the counts in CRIC and CROC are closely coordinated. For example, during initial selection, both counters can be initialized to an all-0's condition. This all-0's condition is then captured, respectively, in the CRIC REG 528 and CROC REG 533 which hold the addresses of all-0's, respectively, for read-in and read-out of main buffer 43 for the first byte of data to be recorded. Then, during such transfer, CRIC and CROC are respectively incremented as just described. If main buffer 43 is full as indicated by the difference between the CRIC and CROC counts, the contents of A REG 464 cannot be written into main buffer 43 and must be held until a register is read out. The full condition of MB 43 is detected by difference circuit 542 and held in MBF (main buffer full) latch 543. MBF 543 is held to the set condition by difference circuit 542 until CROC is advanced. Clock pulses (not shown) from a clock (not shown) continually attempt to reset MBF 543 for enabling AND 539 to send a write request to MB 43.

Data transfers from MB 43 to write or group buffers 45, 48 are in bursts of bytes via gating logic 44. In Figure 2, gating logic 44 is shown as a set of AND's 461. Buffer controls 42 initiate transfer from MB 43. Group buffer 45 includes control circuits (not shown) generating a full (all registers full) and a not-full signal, in any well-known manner. The not-full signal (GB 45 $\overline{\text{FULL}}$) is gated via AND 534 by a gate data signal to line 541. The gated GB 45 $\overline{\text{FULL}}$ signal passes through OR 562 thence AND 557 to send a read buffer request signal to MB 43. AND 557 is enabled to pass GB 45 $\overline{\text{FULL}}$ by the not write cycle request line from inverter 538 and the CRIC not equal CROC signal from compare circuit 550 via the MBMT latch and inverter 596 received over line 536. Priority is assigned to the signal transfer from A REG 464 to MB 43 via NOT or inverter circuit 538 which inhibits AND circuit 557 from passing any read request signals to main buffer 43. A REG 464 being full corresponds to AND 539 being active. In this regard, it will be remembered that transfers of data from write REG 467 into main buffer 43 will not occur until after the MB43WR signal has been supplied over line 511 to write service logic 460. Timing of the various circuits should be such that this first transfer, the size of main buffer 43, and the transfer through scan buffer 40 balance such that there are no interruptions or over-runs of signal data transfers.

The initiation of the record terminator occurs when less than seven bytes to be recorded remain in MB 43. This situation is indicated by the difference in tallies in CRIC and CROC. To this end, difference circuit (subtractor) 542 receives the output signals from CRIC and CROC REG's 528 and 533 and compares same. If the difference between CRIC and CROC counts is greater than six, a full data segment resides in main buffer 43. Whenever difference circuit 542 detects six or fewer bytes of data in main buffer 43, difference circuit 542 then sets "six-or-less" latch 544 initiating generation of the terminator portion of the data record. The activating signal from latch 544 actuates a generator to generate the all-1's end of data marker group, as well as initiating transfer of residual bytes into group buffers 45 and 48, together with the padding bytes. AND 545 supplies the line 103 signal whenever latch 544 is set, AND 534 indicates GB 45 is not full and end of a data segment is indicated on line 104. MBMT latch sends a signal over line 106 signifying that all data has been transferred from MB 43; this action enables padding bytes to fill the residual segment as described in copending application 58902/73 (Serial No. 1452968).

To set MBMT, the contents of CRIC REG 528 and CROC REG 533 are compared by compare circuits 550. If equal, an activating signal is supplied to AND circuit 551. It will be recalled that the CRIC and CROC REG's can be one step behind the counts in CRIC and CROC. Accordingly, even though CRIC and CROC REG's may show an equality, the buffer may not truly be empty. Accordingly, the lowest digit positions of CRIC and CROC are supplied to Exclusive-OR circuit 552 to determine whether or not there is an inequality between these two lowest digit positions thereby signifying that MB 43 readout cycle has not been completed. When completed, Exclusive-OR 552 completes the activation of AND 551 for setting MBMT latch, thereby supplying the MBMT signal over line 106.

Latches 544 and MBMT are used solely for controlling the terminator portion of the data record. A recurring clock pulse from MB 43 resets latches 543, 544, and MBMT upon the start of each MB 43 read or write cycle. A pulse signifying start of a memory cycle operation is generated in accordance with known techniques

The control of transfer of readback signals from buffer register 204 through main buffer 43, scan buffer 41, to CBI is jointly controlled by buffer controls 42 and read service logic 463. CRIC and CROC step the addresses of main buffer 43 similarly to that described for the write operation. In this case, however, CRIC steps up to seven times for enabling main buffer 43 to receive seven consecutive bytes through register 204, while CROC is stepped on a byte-by-byte basis for data transfers through scan buffer 41 to CBI. This action synchronizes the operation of circuits 63 with that of buffer controls 42 and main buffer 43. Circuits 63, when desiring to transfer the burst of seven, supplies the ABC 0-6 signal over line 673 through OR 509. AND 539 passes ABC 0-6 signal on line 673 to AND 557 only when MBF indicates MB 43 is not full. As described for the write or recording operation, AND circuit 557 determines priority between the write request and the read request from read service logic 463 in scan buffer 40.

AND 557 is further responsive to compare circuit 558 indicating no compare between the modulo 32 count and five lower digit positions of CRIC REG 528. Compare 558 is active only during the terminator portion as controlled by AND 559. AND 559 responds to a read forward signal from microprocessor 38, read and TAPE OP on line 313, and end of data signal on line 592 to activate compare 558. That is, comparator 558 supplies an AND circuit activating signal during all times except when the modulo 32 count and CRIC (five bits) compare when the residual and check bit segments are being read back.

Upon seven bytes of data being transferred from circuits 63 to main buffer 43, the ABC 0-6 signal becomes inactive to enable transfers of data bytes accumulated in main buffer 43 to scan buffer 41. ABC 0-6 inactive signal removes the enabling signal from AND 539; thus, enables AND 557 to pass buffer read request signals. NOT circuit 538 responds to the inactive signal of AND 539 to partially enable AND circuit 557. Because the burst of seven data bytes occurs during the ABC cycle, pulses 0-6, there is a break in the request (time ABC-7 plus wait period thereafter) enabling at least several bytes of data to be transferred from main buffer 43 to scan buffer 41 before the next timing period ABC 0-6.

To initiate a transfer to scan buffer 41 from MB 43, AND 562 jointly responds to A REG or B REG not being full signal received over line 563 from AFL (A REG full) latch or BFL (B REG full) latch via OR 508. Either AFL or BFL being reset generates the line 563 signal. AND 562 passes the line 563 signal through OR 562A to AND 557 for generating an MB 43 read request during readback mode. Main buffer 43 acknowledges the request for a read cycle from AND 557 by supplying an MB43RD signal over line 532. This signal pulse passes through tally circuit 531 to increment CROC 474 as described above.

MB43RD pulse signal (Figure 2B) switches the MB 43 supplied signals between A and B REG as main buffer 43 supplies successive bytes of data and as shown in the timing relationships in Figure 2B. The MB43RD timed signal on line 548 passes through AND's 565 or 566 to alternate between the A and B REG's.

AND's 565 and 566 respectively supply register setting signals to A REG 464 and B REG 465 to gate the MB 43 supplied data signals by gates (not shown) within the registers and simultaneously set latches AFL and BFL. The AND's 565 and 566 are alternately successively actuated by AND's 575 and 576, respectively, in response to the then signal states of AFL and BFL latches during the readback mode, as can be readily ascertained by examination of the drawing. In addition to supplying the line 563 A or B REG empty signals, AFL and BFL latches supply coordinating control signals to read service logic 463 for use in control-unit-to-channel communication controls.

Coordination between the channel, scan buffer 41, and main buffer 43 is handled by the read service logic 463. Again, asynchronous logic circuits are used to permit maximum data transfer rates from scan buffer 41 to CBI. The operation is described with respect to a service-in/data-in configuration as was done for recording. The first initial main buffer 43 read cycle sets AFL through AND 565. The A REG full signal partially enables AND 579 in read service logic 463. If SVCO signal 476 is inactive, AND 579 sets RD SVCI latch, RD SVCI being set supplies an enabling signal to AND 570. AND 570 jointly responds to such activating signal, the signal on line 313, plus AND 571 not being active to supply an SVCI signal over line 572, to OR 589, and line 490 connected to an I/O channel (not shown). Since it is desired that the first byte of data be transferred from the A REG, SVCI is activated before DI. Hence, when line 490 SVCI is activated, A REG 464 must begin supplying data signals through OR circuits 574 to CBI in order to be fetched by the CPU or I/O channel (not shown). This function is performed by gates 573 activated by the output of AND 570.

Read service logic 463 alternates between the RD SVCI latch being set and the RD DI (read DATA IN latch) being set as shown in Figure 2B. AND's 570 and 571 cooperate as a latching set of AND's to ensure that either SVCI or DI is sent at one time. In this regard, inverter circuits 577 transfer the outputs of the AND's to the opposite inputs as shown. Both the DI and SVCI latches have identical input circuits.

Read service logic 463 controls AND's 565 and 566 for coordinating setting and resetting AFL and BFL with DO and SVCO. AND 578 responds to SVCI being active and SVCO being active to reset AFL and thereby removes the SVCI signal after A REG 464 signal contents have been transferred to CBI. In a similar manner, AND 581 sets RD DI latch in response to the B REG becoming full. From this it can be seen and from examination of Figure 2B, the asynchronous timing provided by read service logic 463 and the scan buffer empty signal on line 563 coordinate the operation for a maximum data transfer rate between main buffer 43 and CBI.

The two residual counts are used to control proper readback of signals from the magnetic media. The MOD 32 count corresponds to the number or count in CROC REG 533 upon the completion of reading a data record; that is, the data transfer controlled by read service logic 463 must stop when the tally in CROC REG 533 equals the MOD 32 count contained in the residual count byte. In a similar manner, during read backward, data transfer through read service logic 463 must start when a MOD 7 count of segments matches that of a residual MOD 7 count field; that is, the number of data bytes in tape should match that of the actual data transferred to main buffer 43. The MOD 7 count field "initiates" the transfer of data bytes into buffer 43; then the MOD 32 residual count "checks" that it was properly initiated. The residual count field byte containing both the MOD 7 and MOD 32 count fields, when received in REG 204, is gated and AND's 590 to residual byte register 591. The timing pulse ABC-5 jointly with the processor 38 signal on line 592, indicating that the check bit segment is being processed, passes the residual count field byte to register 591. Register 591 supplies the MOD 32 count field signals to comparator 558 wherein it is compared with the CROC REG 533 signal contents. When an equality is found, a deactivating signal is supplied to AND 557 preventing further read cycles from being initiated in main buffer 43 thereby inhibiting further transfer of any signals that may have been written into the buffer. In other words, the last data byte should have been transferred when the two counts are equal. MBMT is set deactivating AND 557 to prevent further data transfers to CBI by read service logic 463.

Referring again to allow CRIC latch 526, the function of compare circuits 524 is most significant on read backward. That is, during read backward, the initially received padding bytes from a residual segment should be discarded. This is done by forcing CRIC not to advance when such padding bytes are being received, i.e., all padding bytes are lodged in register 0 of MB 43.

The first data byte transferred into main buffer 43 from circuits 63 is then overlayed into register 0 for subsequent readout to the I/O channel. Main buffer 43 will not read out any padding bytes since the numerical contents of CRIC equal the numerical contents of CROC; i.e., MBMT latch is active. However, when the appropriate number of padding bytes has been read, as indicated by the MOD 7 count received from register 591 the first data byte is inserted into MB 43. Compare 524 then sets allow CRIC latch 526 to the active condition. The allow CRIC signal then enables CRIC to advance such that the next subsequent data bytes are lodged into register 01, et seq. MBMT latch is reset as previously described to allow buffer readout requests to activate MB 43.

The allow CRIC latch 526 may be reset for each SIO or whenever TAPE OP is supplied to the channel by microprocessor 38. Note that allow CRIC 526 is always set whenever reading is performed in a forward direction.

The MOD 32 count terminates the read operation in either direction of motion.

WHAT WE CLAIM IS:—

1. Digital data processing apparatus in which variable length strings of data signals are transmitted from one location to another in the form of segments of an equal predetermined length including a buffer store to store digital data signals in segment groups, first and second counters to keep a count of data signals entering and leaving the buffer store, and means to determine the end of a string of data signals and to determine whether or not a complete segment has been transmitted depending upon the difference between the counts in the first and second counters.

2. Digital data processing apparatus as claimed in claim 1, including means to generate padding signals whenever an end of a string of data signals is detected and the difference between the first and second counter totals is less than the predetermined length of a segment.

3. Digital data processing apparatus as claimed in claim 1 or claim 2, in which the digital data signals are recorded on a magnetic recording medium and in which the control of signals in the buffer store is substantially as hereinbefore described with reference to Figures 2-1, 2-2, 2A and 2B of the accompanying drawings.

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1454290 COMPLETE SPECIFICATION

5 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1

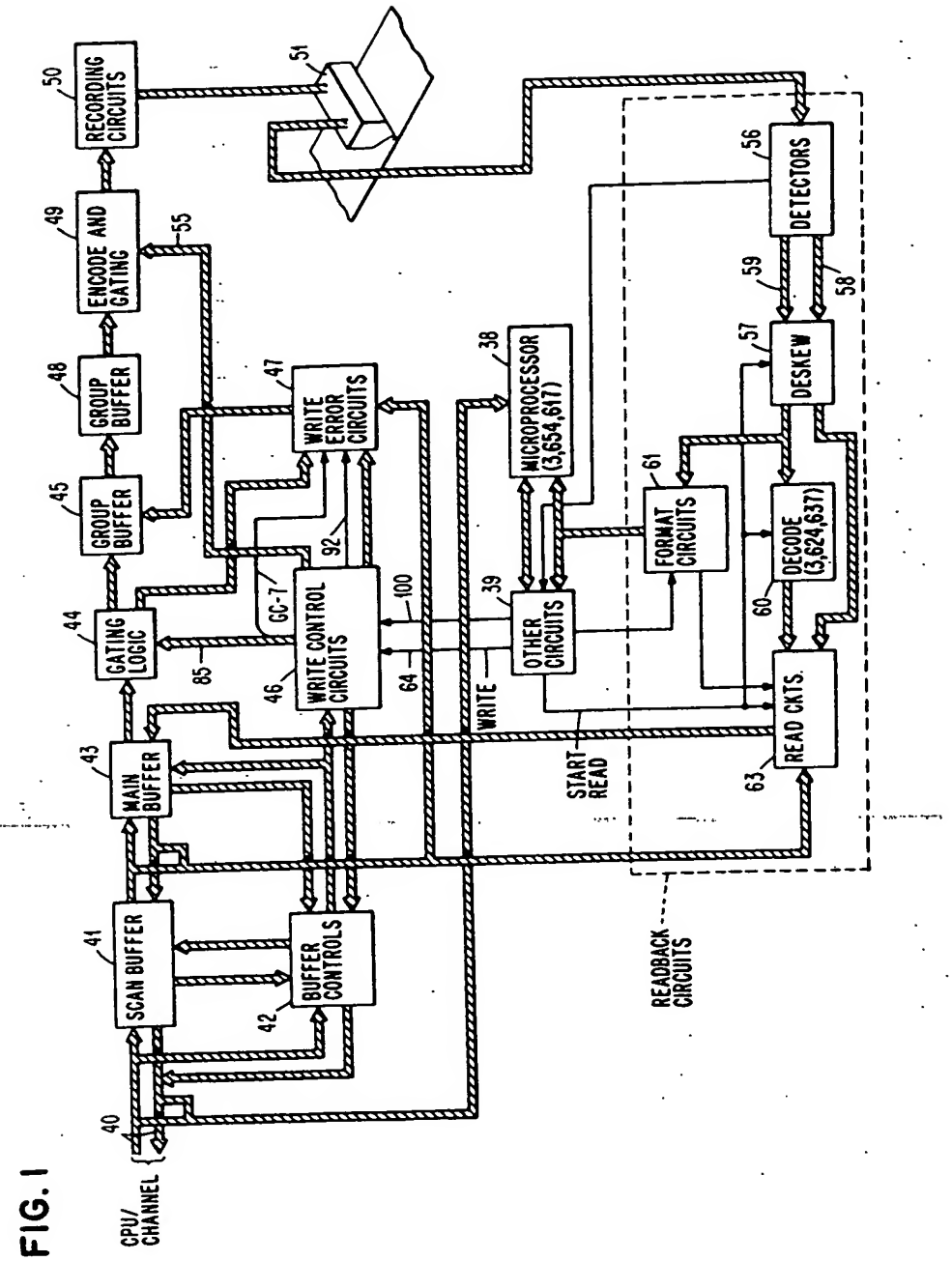


FIG. 1

FIG. 2-1

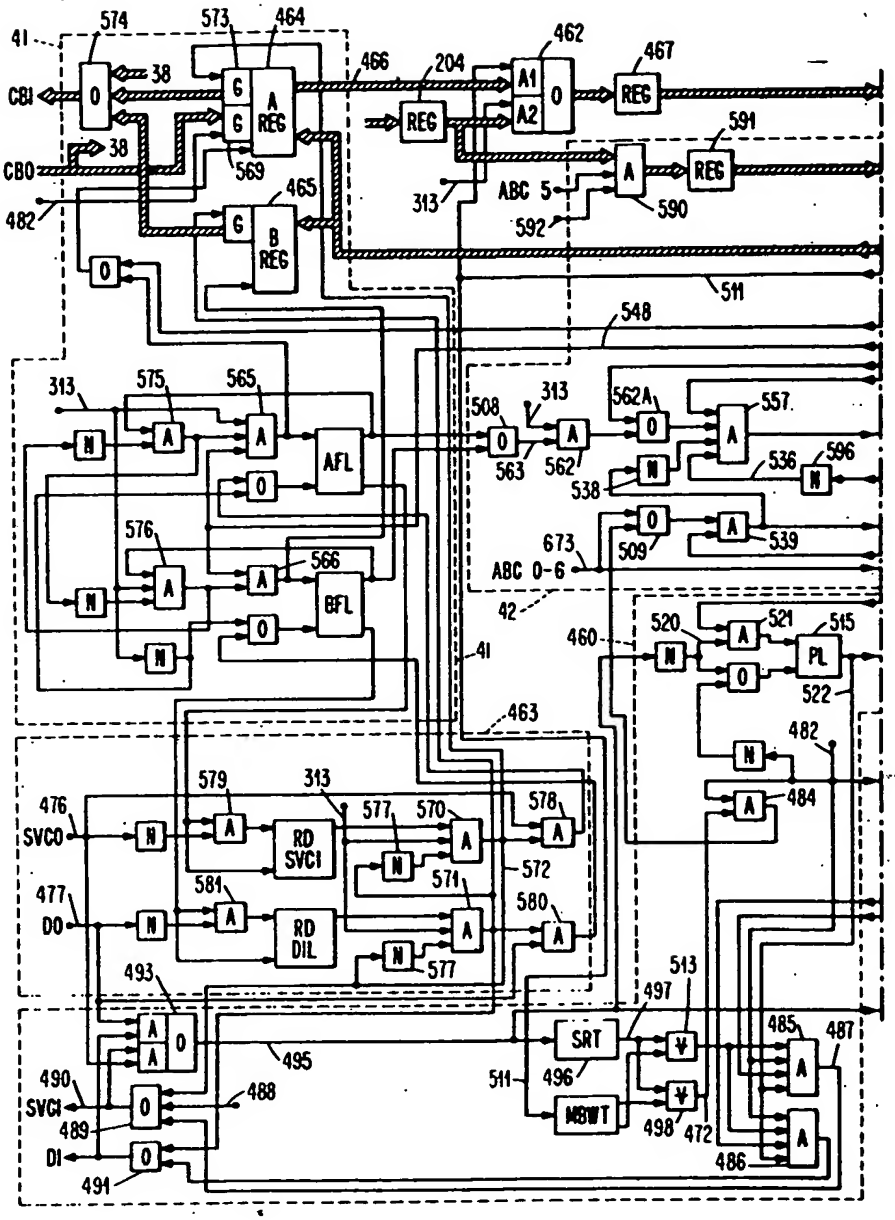
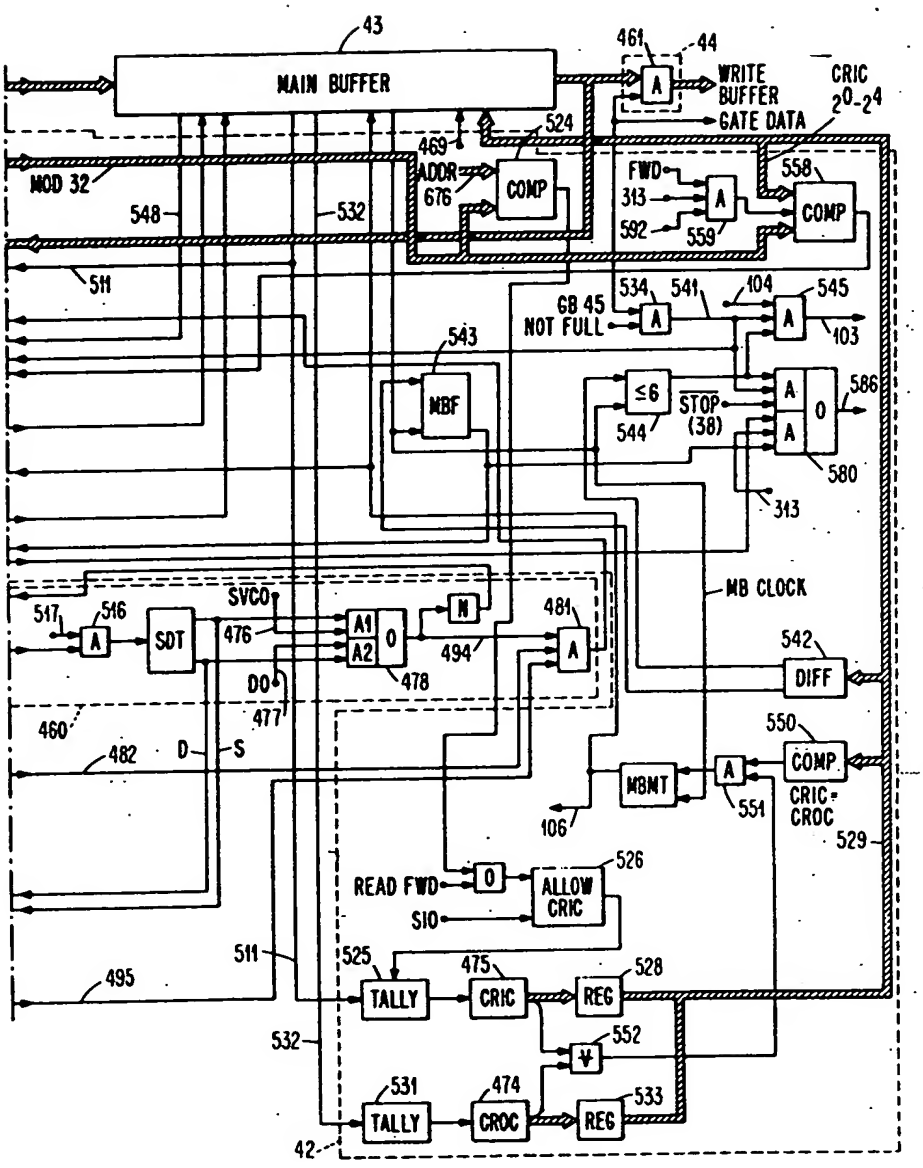
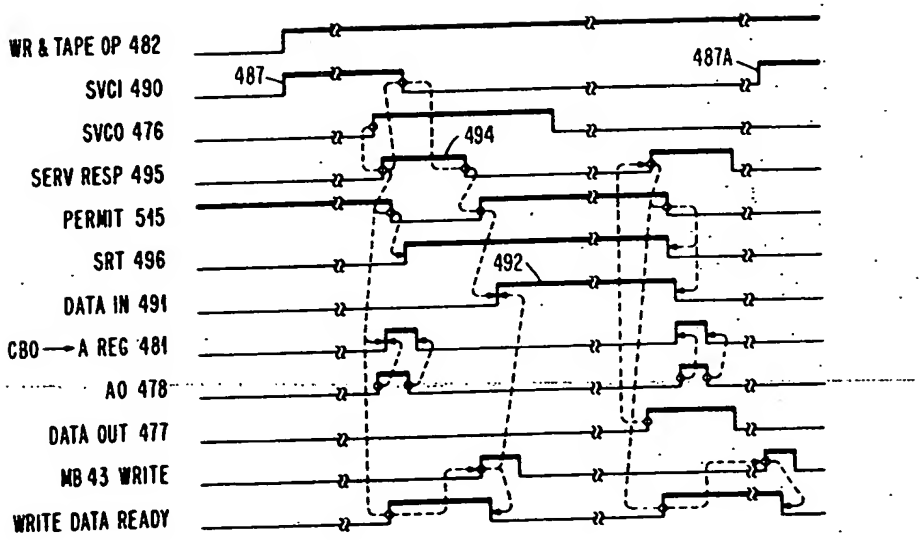

41
574
573
464
CBI
38
CBO
38
482
569
A REG
G
G
466
204
462
467
REG
A1
A2
O
REG
591
313
ABC 5
A
590
REG
592
465
B REG
511
548
313
575
565
AFL
576
566
BFL
508
313
562A
557
563
562
538
536
596
673
ABC 0-6
509
539
42
460
520
521
515
PL
522
463
482
484
476
SVC0
579
313
577
570
578
RD SVCI
572
477
DO
581
571
580
RD DIL
577
493
497
513
485
487
SRT
511
496
MBWT
498
472
495
490
SVCI
488
489
DI
491
486
N
A
O

FIG. 2-2


MAIN BUFFER
WRITE BUFFER
GATE DATA
CRIC 2^0-2^4
MOD 32
ADDR
COMP
FWD
GB 45 NOT FULL
MBF
≤6
STOP (38)
MB CLOCK
SVCO
SDT
DO
DIFF
MBMT
CRIC = CROC
READ FWD
SIO
ALLOW CRIC
TALLY
CRIC
REG
CROC
D
S

1454290 COMPLETE SPECIFICATION
5 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 4

FIG. 2A



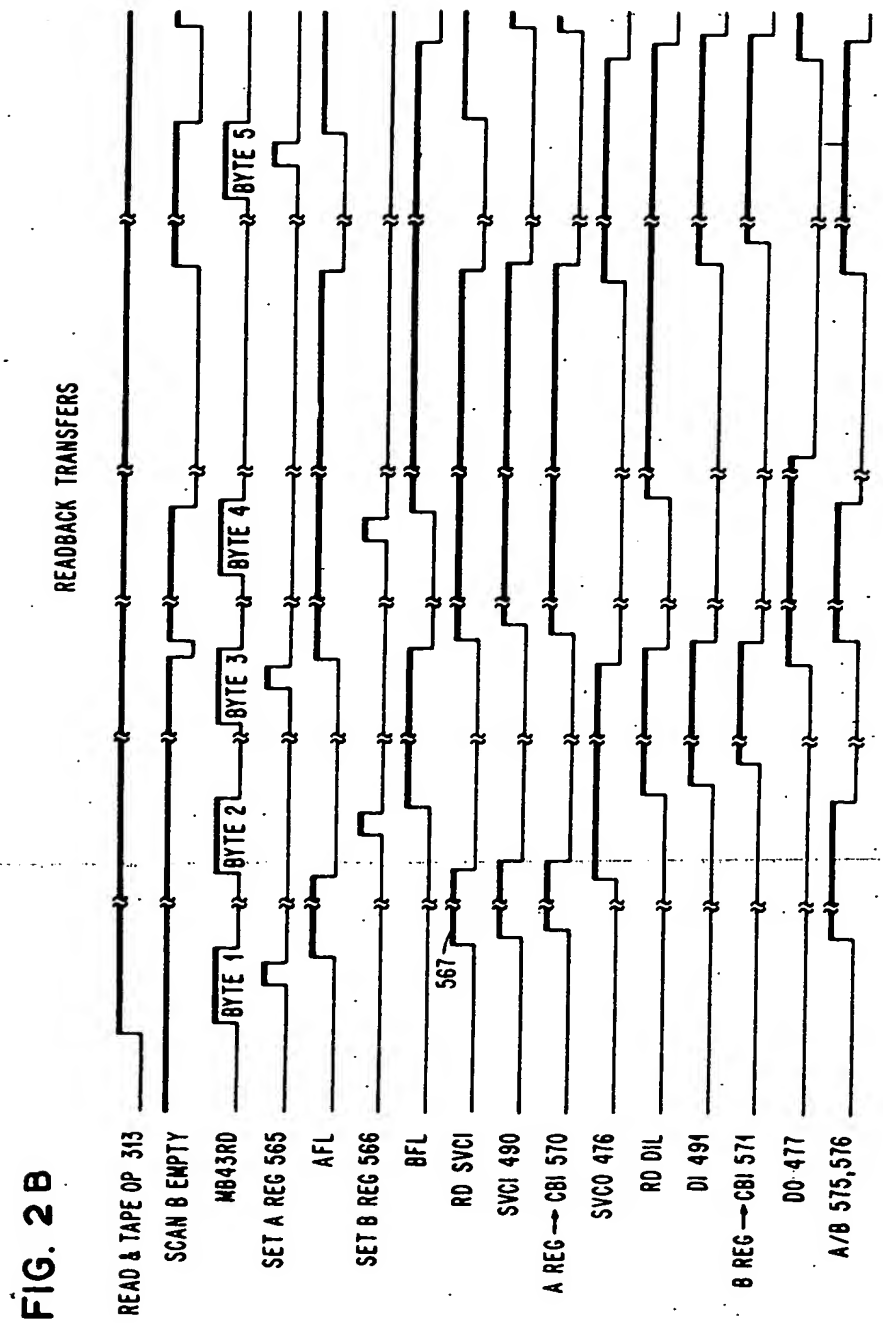

READBACK TRANSFERS
READ & TAPE OP 313
SCAN B EMPTY
MB43RD
BYTE 1
BYTE 2
BYTE 3
BYTE 4
BYTE 5
SET A REG 565
AFL
SET B REG 566
BFL
RD SVCI
567
SVCI 490
A REG → CBI 570
SVCO 476
RD DIL
DI 491
B REG → CBI 571
DO 477
A/B 575,576

FIG. 2B